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FORM PTO-1390 (Modified) (REV 11-2000)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER <b>221109US2PCT</b>	
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371				U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR <b>10/088086</b>	
INTERNATIONAL APPLICATION NO <b>PCT/JP00/06462</b>		INTERNATIONAL FILING DATE <b>21 September 2000</b>		PRIORITY DATE CLAIMED <b>22 September 1999</b>	
TITLE OF INVENTION <b>GRID ARRAY ELECTRONIC COMPONENT, WIRING-STRENGTHENING METHOD AND PRODUCING METHOD THEREOF</b>					
APPLICANT(S) FOR DO/EO/US <b>FUJII Shouichi et al.</b>					
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:					
<ol style="list-style-type: none"> <li>1. <input checked="" type="checkbox"/> This is a <b>FIRST</b> submission of items concerning a filing under 35 U.S.C. 371.</li> <li>2. <input type="checkbox"/> This is a <b>SECOND</b> or <b>SUBSEQUENT</b> submission of items concerning a filing under 35 U.S.C. 371.</li> <li>3. <input checked="" type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.</li> <li>4. <input checked="" type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31).</li> <li>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371 (c) (2)) <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau).</li> <li>b. <input checked="" type="checkbox"/> has been communicated by the International Bureau.</li> <li>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).</li> </ol> </li> <li>6. <input checked="" type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)). <ol style="list-style-type: none"> <li>a. <input checked="" type="checkbox"/> is attached hereto.</li> <li>b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4).</li> </ol> </li> <li>7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)) <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau).</li> <li>b. <input type="checkbox"/> have been communicated by the International Bureau.</li> <li>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</li> <li>d. <input checked="" type="checkbox"/> have not been made and will not be made.</li> </ol> </li> <li>8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).</li> <li>9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).</li> <li>10. <input checked="" type="checkbox"/> An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).</li> <li>11. <input type="checkbox"/> A copy of the International Preliminary Examination Report (PCT/IPEA/409).</li> <li>12. <input checked="" type="checkbox"/> A copy of the International Search Report (PCT/ISA/210).</li> </ol>					
Items 13 to 20 below concern document(s) or information included:					
<ol style="list-style-type: none"> <li>13. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.</li> <li>14. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.</li> <li>15. <input type="checkbox"/> A <b>FIRST</b> preliminary amendment.</li> <li>16. <input type="checkbox"/> A <b>SECOND</b> or <b>SUBSEQUENT</b> preliminary amendment.</li> <li>17. <input type="checkbox"/> A substitute specification.</li> <li>18. <input type="checkbox"/> A change of power of attorney and/or address letter.</li> <li>19. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1 821 - 1.825.</li> <li>20. <input type="checkbox"/> A second copy of the published international application under 35 U.S.C. 154(d)(4).</li> <li>21. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).</li> <li>22. <input type="checkbox"/> Certificate of Mailing by Express Mail</li> <li>23. <input checked="" type="checkbox"/> Other items or information:</li> </ol>					
<b>Notice of Priority/Form PTO-1449</b> <b>PCT/IB/304/Drawings (10 sheets)/PCT/IB/308</b> <b>Amended Sheets (Pages 8, 11, 11A, 17, 17A, 35, 38, and 38A)</b>					

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.492(a)(1)) <b>10/088086</b>		INTERNATIONAL APPLICATION NO. <b>PCT/JP00/06462</b>		ATTORNEY'S DOCKET NUMBER <b>221109US2PCT</b>	
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24. The following fees are submitted: <b>BASIC NATIONAL FEE ( 37 CFR 1.492 (a) (1) - (5) ) :</b> <input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO..... <b>\$1040.00</b> <input checked="" type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO ..... <b>\$890.00</b> <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... <b>\$740.00</b> <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) ..... <b>\$710.00</b> <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) ..... <b>\$100.00</b> <div style="text-align: right;"><b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b></div>				<b>CALCULATIONS PTO USE ONLY</b>  <div style="border: 1px solid black; height: 100px; width: 100%;"></div>																																																																													
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<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">CLAIMS</th> <th style="width: 15%;">NUMBER FILED</th> <th style="width: 15%;">NUMBER EXTRA</th> <th style="width: 15%;">RATE</th> <th style="width: 15%;"></th> <th style="width: 20%;"></th> </tr> </thead> <tbody> <tr> <td>Total claims</td> <td>15 - 20 =</td> <td>0</td> <td>x \$18.00</td> <td></td> <td style="text-align: right;"><b>\$0.00</b></td> </tr> <tr> <td>Independent claims</td> <td>3 - 3 =</td> <td>0</td> <td>x \$84.00</td> <td></td> <td style="text-align: right;"><b>\$0.00</b></td> </tr> <tr> <td colspan="5">Multiple Dependent Claims (check if applicable) <input type="checkbox"/></td> <td style="text-align: right;"><b>\$0.00</b></td> </tr> <tr> <td colspan="5" style="text-align: right;"><b>TOTAL OF ABOVE CALCULATIONS =</b></td> <td style="text-align: right;"><b>\$890.00</b></td> </tr> <tr> <td colspan="5"> <input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.         </td> <td style="text-align: right; vertical-align: bottom;"><b>\$0.00</b></td> </tr> <tr> <td colspan="5" style="text-align: right;"><b>SUBTOTAL =</b></td> <td style="text-align: right;"><b>\$890.00</b></td> </tr> <tr> <td colspan="4">         Processing fee of <b>\$130.00</b> for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).       </td> <td colspan="2" style="text-align: right; vertical-align: bottom;"><b>\$0.00</b></td> </tr> <tr> <td colspan="5" style="text-align: right;"><b>TOTAL NATIONAL FEE =</b></td> <td style="text-align: right;"><b>\$890.00</b></td> </tr> <tr> <td colspan="4">         Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable). <input type="checkbox"/> </td> <td colspan="2" style="text-align: right; vertical-align: bottom;"><b>\$0.00</b></td> </tr> <tr> <td colspan="5" style="text-align: right;"><b>TOTAL FEES ENCLOSED =</b></td> <td style="text-align: right;"><b>\$890.00</b></td> </tr> <tr> <td colspan="5"></td> <td style="text-align: right;">Amount to be: refunded \$</td> </tr> <tr> <td colspan="5"></td> <td style="text-align: right;">charged \$</td> </tr> </tbody></table>				CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE			Total claims	15 - 20 =	0	x \$18.00		<b>\$0.00</b>	Independent claims	3 - 3 =	0	x \$84.00		<b>\$0.00</b>	Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					<b>\$0.00</b>	<b>TOTAL OF ABOVE CALCULATIONS =</b>					<b>\$890.00</b>	<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.					<b>\$0.00</b>	<b>SUBTOTAL =</b>					<b>\$890.00</b>	Processing fee of <b>\$130.00</b> for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).				<b>\$0.00</b>		<b>TOTAL NATIONAL FEE =</b>					<b>\$890.00</b>	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable). <input type="checkbox"/>				<b>\$0.00</b>		<b>TOTAL FEES ENCLOSED =</b>					<b>\$890.00</b>						Amount to be: refunded \$						charged \$
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- a. ☒ A check in the amount of **\$890.00** to cover the above fees is enclosed.
- b. ☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \_\_\_\_\_ to cover the above fees. A duplicate copy of this sheet is enclosed.
- c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030**. A duplicate copy of this sheet is enclosed.
- d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

**NOTE:** Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

**Surinder Sachar**  
**Registration No. 34,423**



**22850**

SIGNATURE

**Marvin J. Spivak**

NAME

**24,913**

REGISTRATION NUMBER

DATE

**March 21 2002**

10/pr13

SPECIFICATION

GRID ARRAY ELECTRONIC COMPONENT, WIRING-STRENGTHENING METHOD  
AND PRODUCING METHOD THEREOF

TECHNICAL FIELD

The present invention relates to a grid array electronic component in which a grid array LSI chip having a large number of lands connected to a wire of a printed wiring board through connecting means is disposed, wherein an auxiliary land is formed on a connection portion between the wire and a land of the printed wiring board corresponding to the land of the corner portion of the grid array LSI chip. The invention also relates to a wire strengthening method.

BACKGROUND TECHNIQUE

As shown in Fig.18(A), in a conventional grid array electronic component, a via hole B of a printed wiring board K and a land L of the printed wiring board K corresponding to a large number of lands of a grid array LSI chip P mounted on the printed wiring board K are directly connected to each other through a wiring pattern H.

In a conventional wiring board having the lands (Japanese Patent Application Laid-open No.H8-213730 (improvement of a break caused by fracture based on difference of thermal expansion), Japanese Utility Model Application Laid-open Nos.S61-201374 and S62-184783 (improvement of land shape in accordance with high density of wire), Japanese Patent Publication No.S56-22151, and the like), as shown in Fig.19, an auxiliary land AL is formed on a portion of a periphery or

an entire periphery of through holes TH, and even if the through holes TH are deviated from each other, connection properties are secured.

In a conventional printed wiring board (Japanese Patent Applications Laid-open Nos. H1-115195, H11-54859 and S64-84875, as well as Japanese Patent No. 2519068), since there is a problem that if a tier drop is added to secure electrical conduction of a land in a printed board of epoxy glass or the like and to avoid a danger of break of wire, the entire area of the land is increased and thus, density cannot be increased as compared with a case in which the tier drop is not added, a predetermined insulation gap cannot be obtained between the tier drop and another conductive circuit. Therefore, tier drops TD are offset with respect to a land L1, and the tier drops TD are formed on one side of a line or asymmetrically in a lateral direction as shown in Fig.20.

In a mounting structure of a conventional ball grid array package (Japanese Patent Application Laid-open No. H10-335516), as shown in Fig.21, in order to prevent thermal fatigue life of soldering from being lowered by reduction bonding force of soldering based on void caused by air trapped in the four corner via holes BH of the disposition region of a rectangular ball grid array package, flat pads PP are disposed instead of a pad BH for the via hole.

In the conventional grid array electronic component, the via hole B of the printed wiring board K and the land L of the printed wiring board K corresponding to a large number of lands of the grid array LSI chip P mounted on the printed wiring board K are directly connected to each other through the wiring pattern H. Therefore, if a load is applied to the printed wiring board

K, a brake is generated in the wiring pattern H.

That is, if warpage and distortion are generated in the printed wiring board K, a great stress is applied to a connection portion between the wiring pattern H, the via hole B of the printed wiring board K and the land L of the printed wiring board K corresponding to the land of the grid array LSI chip. Therefore, a brake is generated in the connection portion of the wiring pattern H.

As shown in Fig.19, the conventional wiring board having the land, the through holes TH are formed at a portion of its periphery or an entire periphery with an auxiliary land AL, and even if the through holes TH are offset from each other, the connection properties are obtained. Therefore, this is a technique related to a 2.54 mm pin grid array (PGA) between pins, and this is not a technique related to BGA of ball grid array LSI chip in which a large number of soldering balls having 1.27 mm pitch between pins are disposed on a lower surface of an LSI device.

In the conventional printed wiring board, if the tier drop is added to moderate the concentration of stress of the land of the printed board of epoxy glass or others of 1 mm thickness, the entire area of the land is increased. Therefore, there are problems that the density is not increased as compared with a case in which the tier drop is not added, and a predetermined insulation distance between the tier drop and other conductive circuit cannot be secured. Thus, the tier drops TD are decentered with respect to the land L1, and are formed on one side of the line or asymmetrically in the lateral direction, and two leads D1 and D2 are interposed between adjacent lands L1 and L2, and this technique is judged as being one generation older technique

of the ball grid array (BGA) in which a large number of surface-mounting type soldering balls of 1.27 mm pitch are disposed on a lower surface of the LSI device.

Further, in the conventional printed wiring board, since a brake of the wiring pattern when a load is applied to the printed wiring board to which the ball grid array type LSI chip is mounted is not prevented, the printed wiring board is different in wiring pattern and the like of the pitch, lead and the like of the land of the LSI device and printed board which is soldered to the printed board.

In the mounting structure of the conventional ball grid array package, a flat pad PP is disposed instead of a via hole pad BH in order to avoid reduction of the soldering thermal fatigue life caused by reduction of the soldering bonding force based on void by air trapped in four corner via holes BH in disposition region of the rectangular ball grid array package, and a brake of the wiring pattern when a load is applied to the printed wiring board to which the ball grid array type LSI chip is mounted is not prevented. Therefore, the land whose wiring pattern is broken is not provided with an auxiliary land naturally.

#### DISCLOSURE OF THE INVENTION

Thereupon, the present inventor analyzed a wire failure caused by a brake of wiring pattern of the printed wiring board to which the ball grid array type LSI chip shown in Fig.18(A) was mounted, and found that the brake was generated in a correction step which corrected warpage and distortion of the printed wiring board which was generated in a reflow soldering step, or in an assembling step of the printed wiring board.

Further, the present inventor found that a portion where

the brake was generated was a region of about 1 mm of the connection portion C between the land L and the wiring pattern P as shown in Fig.18(B), and a region where a brake of the ball grid array type LSI chip was generated was a region (portion) where an excessive tensile stress was applied between the land of the printed wiring board such as a corner portion of the ball grid array type LSI chip or an end of an IC chip and a wiring pattern as the connecting means.

It is assumed that the wire failure is caused in such a manner that warpage and distortion are generated in the printed wiring board by heating and a weight of the ball grid array type LSI chip itself when the latter is soldered and bonded to the printed wiring board, and when the warpage and distortion of the printed wiring board are corrected, the correction amount or a stress becomes maximum in the corner portion of the ball grid array type LSI chip or an end of the IC chip, and an excessive stress is applied to the connection portion between the land and the wiring pattern in order to break the wiring pattern. It is assumed that a brake of the wiring pattern caused when an excessive load is applied to the printed wiring board in the assembling step of the printed wiring board is generated by the same reason.

Thereupon, the inventor reached the present invention in which an auxiliary land is formed in the connection portion of a land connecting to a wiring pattern at a portion where an excessive stress is applied between the land of the printed wiring board and the wiring pattern as the connecting means when a load is applied to the printed wiring board.

Further, the inventor paid attention to a technical idea of the present invention in which in a grid array electronic







LSI chip having a large number of lands connected to a large number of lands through connecting means, the latter lands are connected to a wire of a printed wiring board, wherein an auxiliary land is formed at a connection portion of the land connecting a wiring pattern at portions where an excessive tensile stress is applied between the lands in the printed wiring board corresponding to the grid array LSI chip and the wiring pattern as the wire.

The grid array electronic component of the present invention (the second invention set forth in claim 2), according to claim 1, wherein the auxiliary land is formed at the land located on at least a portion where an excessive tensile stress as compared with another portion of the printed wiring board is applied when a load is applied to the printed wiring board.

The grid array electronic component of the present invention (the third invention set forth in claim 3), according to claim 2, wherein the auxiliary land is formed at the land located on a portion corresponding to a corner portion of the grid array LSI chip in the printed wiring board.

The grid array electronic component of the present invention (the fourth invention set forth in claim 4), according to claim 2, wherein the auxiliary land is formed at the land located on a portion corresponding to an end of an IC chip disposed in the grid array LSI chip in the printed wiring board.

The grid array electronic component of the present invention (the fifth invention set forth in claim 5), according to claim 2, wherein the auxiliary land is formed at the land connected to the wiring pattern which is formed in a direction in which a warpage of the printed wiring board is generated and in a direction closer to the former direction in a reflow soldering

step of the grid array electronic component.

The grid array electronic component of the present invention (the sixth invention set forth in claim 6), according to claim 2, wherein the auxiliary land is formed at the land in which an excessive tensile stress is applied to the wiring pattern in a correcting step which corrects warpage and distortion of the printed wiring board or an assembly step.

The grid array electronic component of the present invention (the seventh invention set forth in claim 7), according to claim 2, wherein the auxiliary land is formed so that a connection cross section area from the land of the printed wiring board corresponding to the portion of the land of the grid array LSI chip to the wiring pattern is gradually varied.

The grid array electronic component of the present invention (the eighth invention set forth in claim 8) according to claim 3, wherein the auxiliary land is constituted by an auxiliary land having a different shape in accordance with a position of the land of the printed wiring board corresponding to the land of the corner portion of the grid array LSI chip.

The grid array electronic component of the present invention (the ninth invention set forth in claim 9), according to claim 3, wherein the auxiliary land is constituted so that an average value of a connection cross section area of a land closer to the printed wiring board corresponding to the land closer to an end of the corner portion of the grid array LSI chip becomes larger.

The grid array electronic component of the present invention (the tenth invention set forth in claim 10), according to claim 2, wherein the auxiliary land is formed at a connection portion around a through hole connected to the wiring pattern on an inner

layer printed wiring board of a multilayer printed wiring board constituting the printed wiring board.

The grid array electronic component of the present invention (the eleventh invention set forth in claim 11), according to claim 3, wherein the wiring pattern connected to the land formed with the auxiliary land of the printed wiring board corresponding to a corner portion of the grid array LSI chip is connected to a connection portion formed with an auxiliary land of a via hole on the printed wiring board.

A wire strengthening method of the present invention (the twelfth invention set forth in claim 12) which connects a printed wiring board constituting a grid array electronic component and a grid array LSI chip mounted to the printed wiring board, wherein

an auxiliary land is formed at a connection portion between the wire and a land of the printed wiring board corresponding to a land of a corner portion of the grid array LSI chip, thereby strengthening the connection portion of the wire.

The wire strengthening method of the present invention (the thirteenth invention set forth in claim 13), according to claim 12, wherein the connection portion of the wire is strengthened by forming the auxiliary land at the connection portion of the wire of a via hole of the printed wiring board.

A producing method of a grid array electronic component of the present invention (the fourteenth invention set forth in claim 14) for connecting a printed wiring board constituting a grid array electronic component and a grid array LSI chip mounted to the printed wiring board to each other through a wiring pattern, wherein the grid array electronic component having a strengthened connection portion of the wiring pattern is produced by forming an auxiliary land at a connection portion between the wire and

a land of the printed wiring board corresponding to a land of a corner portion of the grid array LSI chip.

The producing method of a grid array electronic component of the present invention (the fifteenth invention set forth in claim 15), according to claim 14, wherein the grid array electronic component having the strengthened connection portion of the wire is produced by forming the auxiliary land on the connection portion of the wire and the via hole on the printed wiring board.

A grid array electronic component of the present invention (the sixteenth invention set forth in claim 16) in which a grid array LSI chip having a large number of lands connected to a large number of lands through connecting means, the latter lands are connected to a wire of a printed wiring board, wherein an auxiliary land whose connection cross section area is increased is formed on a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress is applied in a producing step between a land in a printed wiring board corresponding to the grid array LSI chip and the wiring pattern which is taken outward to be connected to a via hole as the wire.

A grid array electronic component of the first invention having the above-described construction, in which a grid array LSI chip having a large number of lands connected to a large number of lands through connecting means, the latter lands are connected to a wire of a printed wiring board, wherein an auxiliary land is formed on a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress is applied between the lands in the printed wiring board corresponding to the grid array LSI chip and the wiring pattern as the wire.

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Therefore, the present invention provides the effect that by moderating the concentration of stress on the connection portion a break of the wiring pattern in the connection portion is prevented.

The grid array electronic component of the second invention having the above-described construction, according to the first invention, wherein the auxiliary land is formed at the land located on at least a portion where an excessive tensile stress as compared with another portion of the printed wiring board is applied when a load is applied to the printed wiring board. The present invention exhibits the effect that at least

concentration of stress on the connection portion of the land connecting to the wiring pattern at the portion where an excessive tensile stress is applied is moderated, thereby preventing a brake of the wiring pattern in the connection portion.

The grid array electronic component of the third invention having the above-described construction, according to the second invention, wherein the auxiliary land is formed on the land located on a portion corresponding to a corner portion of the grid array LSI chip in the printed wiring board, where an excessive tensile stress as compared with another portion of the printed wiring board is applied when a load is applied to the printed wiring board.

Therefore, the present invention provides the effect that a brake of the wiring pattern in the connection portion is prevented by moderating the concentration of stress on the connection portion of the land located on a portion corresponding to a corner portion of the grid array LSI chip on the printed wiring board.

The grid array electronic component of the fourth invention having the above-described construction, according to the second invention, wherein the auxiliary land is formed on the land located on a portion corresponding to an end of an IC chip disposed in the grid array LSI chip on the printed wiring board.

Therefore, the present invention provides the effect that a brake of the wiring pattern in the connection portion is prevented by moderating the concentration of stress on the connection portion between the printed pattern and the land located on a portion corresponding to an end of an IC chip on the printed wiring board.

The grid array electronic component of the fifth invention

having the above-described construction, according to the second invention, wherein the auxiliary land is formed at the land connected to the wiring pattern which is formed in a direction in which a warpage of the printed wiring board is generated and in a direction closer to the former direction in a reflow soldering step of the grid array electronic component.

Therefore, the present invention provides the effect that a break of the wiring pattern in the connection portion is prevented by moderating the concentration of stress on the connection portion between the printed pattern and the land where the excessive tensile stress is applied corresponding to the warpage of the printed wiring board.

The grid array electronic component of the sixth invention having the above-described construction, according to the second invention, wherein the auxiliary land is formed at the land in which an excessive tensile stress is applied to the wiring pattern in a correcting step which corrects warpage and distortion of the printed wiring board or an assembly step.

Therefore, the present invention provides the effect that a break of the wiring pattern in the connection portion is prevented by moderating the concentration of stress on the connection portion between the printed pattern and the land where the excessive tensile stress is applied to the wiring pattern in the correcting step or the assembly step.

The grid array electronic component of the seventh invention having the above-described construction, according to the second invention, wherein the auxiliary land is formed so that a connection cross section area from the land of the printed wiring board corresponding to the portion of the land of the grid array LSI chip to the wiring pattern is gradually



varied.

Therefore, the present invention exhibits the effect that a brake of the wiring pattern in the connection portion is reliably prevented by moderating effectively the concentration of stress on the connection portion when warpage and distortion are generated in the printed wiring board.

The grid array electronic component of the eighth invention having the above-described construction, according to the third invention, wherein the auxiliary land is constituted by an auxiliary land having a different shape in accordance with a position of the land on the printed wiring board corresponding to the land of the corner portion of the grid array LSI chip.

Therefore, the present invention exhibits the effect that a brake of the wiring pattern in the connection portion is prevented by moderating the concentration of stress on the connection portion and by determining the shape of the auxiliary land in consideration of the tensile stress applied to the connection portion between the wiring pattern and the land of the corner portion of the grid array electronic component as well as a shape of the pattern on the printed wiring board.

The grid array electronic component of the ninth invention having the above-described construction, according to the third invention, wherein the auxiliary land is constituted so that an average value of a connection cross section area of a land closer to the printed wiring board corresponding to the land closer to an end of the corner portion of the grid array LSI chip becomes larger.

In the present invention, since the auxiliary land includes a cross section for connection of an average value in accordance with the stress applied to the connection portion when a load

is applied to the printed wiring board, the strength of the lands of the corner portion are uniformed, and reliability is enhanced.

The grid array electronic component of the tenth invention having the above-described construction, according to the second invention, wherein the auxiliary land is formed at a connection portion around a through hole connected to the wiring pattern on an inner layer printed wiring board of a multilayer printed wiring board constituting the printed wiring board.

The present invention exhibits the effect that a brake of the wiring pattern in the connection portion is prevented by moderating the concentration of stress of the connection portion between the wiring pattern and the through hole on the inner layer printed wiring board of the multilayer printed wiring board.

The grid array electronic component of the eleventh invention having the above-described construction, according to the third invention, wherein the wiring pattern connected to the land formed with the auxiliary land of the printed wiring board corresponding to a corner portion of the grid array LSI chip is connected to a connection portion formed with an auxiliary land of a via hole on the printed wiring board.

The present invention prevents a brake of the wire in the connection portion of the via hole of the printed wiring board by moderating the concentration of stress of the connection portion of the via hole of the printed wiring board when the load is applied to the printed wiring board.

A wire strengthening method of a wire of the twelfth invention having the above-described construction, which connects a printed wiring board constituting a grid array electronic component and a grid array LSI chip mounted to the

[illegible]

The present invention prevents a brake of wiring pattern of one end of the printed wiring board on the side of the land. The wire strengthening method of the thirteenth invention having the above-described construction, according to the twelfth invention, wherein the connection portion of the printed wiring board of the wire on the side of the via hole is also strengthened by forming the auxiliary land at the connection portion of the via hole on the printed wiring board connecting the wire and thus, there is effect that brakes on the opposite ends of the wire are prevented.

A producing method of a grid array electronic component of the fourteenth invention having the above-described construction for connecting a printed wiring board constituting a grid array electronic component and a grid array LSI chip mounted to the printed wiring board to each other through a wiring pattern, wherein the grid array electronic component having a strengthened connection portion of the wiring pattern at the side of the land on the printed wiring board is produced by forming an auxiliary land at a connection portion between the wire and a land on the printed wiring board corresponding to a land of a corner portion of the grid array LSI chip.

The producing method of a grid array electronic component of the fifteenth invention having the above-described construction, according to the fourteenth invention, wherein the grid array electronic component having the strengthened

connection portion of the wire at the side of the via hole on the print wiring board is produced by forming the auxiliary land at the connection portion of the wire and the via hole on the printed wiring board.

A grid array electronic component of the sixteenth invention having the above-described construction in which a grid array LSI chip having a large number of lands connected to a large number of lands through connecting means, the latter lands are connected to a wire of a printed wiring board, wherein an auxiliary land whose connection cross section area is increased is formed on a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress is applied in a producing step between a land in a printed wiring board corresponding to the grid array LSI chip and the wiring pattern which is taken outward to be connected to a via hole as the wire.

Therefore, the invention exhibits the effect that by moderating the concentration of stress of the connection portion the break of the wire of the wiring pattern at the connection portion is prevented.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a plan view showing a portion of a printed wiring board to which a grid array LSI chip of a first embodiment is mounted;

Fig.2 is a sectional view showing a state in which the grid array LSI chip of the first embodiment is mounted to a printed wiring board;

Fig.3 is a sectional view taken along a line A-A in Fig.1 showing a state in which the grid array LSI chip of the first embodiment is assembled on the printed wiring board;

$\begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \\ 17 \\ 18 \\ 19 \\ 20 \\ 21 \\ 22 \\ 23 \\ 24 \\ 25 \\ 26 \\ 27 \\ 28 \\ 29 \\ 30 \\ 31 \\ 32 \\ 33 \\ 34 \\ 35 \\ 36 \\ 37 \\ 38 \\ 39 \\ 40 \\ 41 \\ 42 \\ 43 \\ 44 \\ 45 \\ 46 \\ 47 \\ 48 \\ 49 \\ 50 \\ 51 \\ 52 \\ 53 \\ 54 \\ 55 \\ 56 \\ 57 \\ 58 \\ 59 \\ 60 \\ 61 \\ 62 \\ 63 \\ 64 \\ 65 \\ 66 \\ 67 \\ 68 \\ 69 \\ 70 \\ 71 \\ 72 \\ 73 \\ 74 \\ 75 \\ 76 \\ 77 \\ 78 \\ 79 \\ 80 \\ 81 \\ 82 \\ 83 \\ 84 \\ 85 \\ 86 \\ 87 \\ 88 \\ 89 \\ 90 \\ 91 \\ 92 \\ 93 \\ 94 \\ 95 \\ 96 \\ 97 \\ 98 \\ 99 \\ 100 \end{array}$

Fig. 4 is a plan view showing a portion of the printed wiring board to which a grid array LSI chip of a second embodiment of the present invention is mounted and showing a wire strengthening method;

Fig.5 is a sectional view taken along a line B-B in Fig.4 showing a state in which the grid array LSI chip of the second embodiment is assembled on the printed wiring board;

Fig.6 is a partially enlarged plan view showing a portion of a printed wiring board to which a grid array LSI chip of a third embodiment of the invention is mounted;

Fig.7 is a partially enlarged plan view showing a portion of a printed wiring board to which a grid array LSI chip of a fourth embodiment of the invention is mounted;

Fig.8 is a plan view showing a portion of a printed wiring board to which a grid array LSI chip of a fifth embodiment of the invention is mounted;

Figs.9 are explanatory views for explaining steps from a mounting operation of the grid array LSI chip of the fifth embodiment to the printed wiring board to an assembling operation;

Fig.10 is a plan view showing a printed wiring board to which a grid array LSI chip of a sixth embodiment of the invention is mounted;

Fig.11 is a front view showing a state in which a printed wiring board to which a grid array LSI chip of a seventh embodiment of the invention is mounted is warped, as viewed from front side of an in-circuit tester;

Fig.12 is a front view of showing a state of an in-circuit tester of a printed wiring board to which the grid array LSI chip of the seventh embodiment is mounted, as viewed from front side;

Fig.13 is a sectional view showing an inner structure of a multilayer printed wiring board to which a grid array LSI chip of an eighth embodiment of the invention is mounted;

Fig.14 is a partial plan view showing lands, wiring pattern and via holes on the printed wiring board of a first layer of the eighth embodiment;

Fig.15 is a partial plan view showing a wiring pattern and a via hole on a second layer printed wiring board of the eighth embodiment;

Fig.16 is a partial enlarged view showing a shape of another auxiliary land of the present invention;

Fig.17 is a sectional view showing an inner structure of a multilayer printed wiring board to which a grid array LSI chip of a modification of the eighth embodiment of the invention is mounted;

Figs.18 are plan views showing a printed wiring board to which a conventional grid array LSI chip is mounted;

Fig.19 is a partial plan view showing a wiring board having a conventional land;

Fig.20 is a partial plan view showing a conventional printed wiring board; and

Fig.21 is a partial sectional view showing a mounting structure of a conventional ball grid array package.

#### BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment of the present invention will be explained below using the drawings.

##### (First Embodiment)

As shown in Figs.1 to 3, in a grid array electronic component of a first embodiment in which a grid array LSI chip 2 having a large number of lands 3 connected to a large number of lands 13 through connecting means 30, the lands 13 are connected to a wire 4 of a printed wiring board 1, an auxiliary land 5 is formed at a connection portion 31 of the lands 13 on the printed wiring board 1 corresponding to the lands 3 of a corner portion of the grid array LSI chip 2 connecting the wire 4.

As shown in Fig.2, in the first embodiment, a ball grid array LSI chip in which soldering balls 30 as the connecting means 30 disposed on the lands 3 which are arranged in a form of grid is used as the grid array LSI chip 2 for one sample. As the grid array LSI chip 2, a chip size package including Super CSP of a KGD package capable of being mounted to a surface which realized a real chip size in which the soldering ball is disposed

directly on a silicon wafer can be employed other than the ball grid array LSI chip.

The spherical soldering ball 30 as the connecting means 30 disposed on the lands 3 arranged in the form of grid in the ball grid array LSI chip constituting the grid array LSI chip 2 is deformed in a form of tabor as shown in Fig.3, and the soldering ball 30 and the lands 13 of the printed wiring board 1 corresponding to the lands 3 of the ball grid array LSI chip are welded and electrically connected to each other.

As shown in Fig.1, a connection cross section area of a tier drop constituting the auxiliary land 5 is gradually reduced, i.e., is formed into a fan-like shape from the lands 3 of a right upper corner portion of the grid array LSI chip 2 which is shown in detail as representative to a wiring pattern constituting the wire 4.

As shown in Fig.3, the wiring pattern constituting the wire 4 is connected to a via hole 14 formed in the printed wiring board 1, and a resist 15 is applied to an upper portion of the via hole 14.

As shown in Fig.1, the reinforcing tier drop constituting the auxiliary land 5 is constituted by an auxiliary land of different shape and size in accordance with a position of the land 13 on the printed wiring board 1 corresponding to the land 3 of the corner portion of the grid array LSI chip 2.

That is, the tier drop constituting the auxiliary land 5 is formed so that an average value of its connection cross section area becomes larger as closer to the land 13 of the printed wiring board 1 corresponding to the land 3 closer to an end of the corner portion of the grid array LSI chip 2, and the tier drop formed in the land 13 corresponding to a position closer



to the corner portion has wider width and longer length in the longitudinal direction.

According to the grid array electronic component of the first embodiment having the above structure, in the grid array electronic component in which the grid array LSI chip 2 connected to the printed wiring board 1 through the large number of lands 13 and the wire is disposed, the tier drop constituting the auxiliary land 5 is formed at the connection portion 31 of the wiring pattern constituting the wire 4 of the lands 13 on the printed wiring board 1 corresponding to the lands 3 of the corner portion of the grid array LSI chip 2. Therefore, a load is applied to the printed wiring board 1 in a correction step which corrects warpage of the printed wiring board 1 and an assembly step when warpage and distortion are generated in the printed wiring board 1 in a reflow soldering step, concentration of stress of the connection portion 31 when the tensile stress is applied to the connection portion 31 between the lands 3 and the wire 4 is moderated.

To moderate the concentration of stress of the connection portion 31 when the tensile stress is applied is to increase the area (cross section area) of the connection portion 31 to which the tensile stress is applied by forming the auxiliary land 5 whose width is gradually reduced in its longitudinal direction on the connection portion 31 between the lands 3 and the wire 4, and to reduce the tensile stress which is applied per unit area, thereby preventing a great tensile stress from being applied locally, and to strengthen the connection portion 31 by eliminating abrupt variation in area (cross section area) of the connection portion 31 and by eliminating abrupt variation in tensile stress so that the brake is not generated easily even



the land 3 of the corner portion of the grid array LSI chip 2, the shape is determined in consideration of the tensile stress applied to the corner portion between the land and the wiring pattern in the corner portion of the grid array electronic component as well as the pattern shape of the printed wiring board corresponding to the corner portion of the grid array electronic component, and the concentration of stress of the connection portion 31 is moderated, thereby providing the effect that the brake of the wire in the connection portion 31 is prevented.

According to the grid array electronic component of the first embodiment, the tier drop constituting the auxiliary land 5 is constituted so that its average value of the connection cross section area is greater as closer to the land 13 of the printed wiring board 1 corresponding to the land close to the end of the corner portion of the grid array LSI chip 2. Therefore, since the tier drop constituting the auxiliary land 5 includes the connection cross section area of average value in accordance with the stress applied to the connection portion 31 when the load is applied to the printed wiring board 1, there is effect that the strength of the lands 13 of the printed wiring board 1 corresponding to the corner portion is uniformed, and the reliability is enhanced.

#### (Second Embodiment)

As shown in Figs. 4 and 5, a grid array electronic component, a producing method and a wire strengthening method of a second embodiment are different from those of the first embodiment in that an auxiliary land 51 is also formed at the via hole 14 of the printed wiring board 1, and the difference will be mainly

explained below.

As shown in Figs.4 and 5, in the grid array electronic component of the second embodiment, the wire 4 (pattern) connected to the land 13 formed with the semi-circular auxiliary land 5 of the printed wiring board 1 corresponding to the corner portion of the grid array LSI chip 2 is connected to the connection portion 32 formed with the semi-circular auxiliary land 51 in the via hole 14 of the printed wiring board 1.

According to the wire strengthening method and the producing method of grid array electronic component according to the second embodiment, in which on the wire 4 connected the printed wiring board 1 and the grid array LSI chip 2 mounted to the printed wiring board 1, the auxiliary land 5 is formed at the connection portion 31 between the wire 4 and the land 13 on the printed wiring board 1 corresponding to the land 3 of the corner portion of the grid array LSI chip 2, the auxiliary land 51 is formed on the connection portion 32 between the wire 4 and the via hole 14 of the printed wiring board 1, thereby strengthening the connection portion 32 of the wire pattern 4, and thereby producing the grid array electronic component having the strengthened connection portion 32 of the wire pattern 4.

In the grid array electronic component of the second embodiment having the above structure, the wire 4 connected to the auxiliary land 3 formed at the land 13 of the printed wiring board 1 corresponding to the land 3 of the corner portion of the grid array LSI chip 2 is connected to the connection portion 32 formed with the auxiliary land 51 of the via hole 14 on the printed wiring board 1. Therefore, the concentration of stress of the connection portion 32 of the via hole 14 on the printed wiring board 1 when a load is applied to the printed wiring board





patterns 4 in the connection portions 31 are prevented.

(Fourth Embodiment)

As shown in Fig.7, the grid array electronic component of a fourth embodiment is different from that of the third embodiment in that the wiring patterns 4 are taken inward radially from the lands 13 in the printed wiring board 1 corresponding to the lands 3 of the four corner portions of the frame-like grid array LSI chip 2, and the difference will be mainly explained below.

That is, the auxiliary land 5 is formed on the connection portion 31 between the land 13 and the wire pattern 4 which is taken inward radially from the land 13 of the corner portion of the frame-like grid array LSI chip 2 and which is connected to a central trough hole (not shown).

According to the grid array electronic component of the fourth embodiment having the above structure, since the tier drop constituting the auxiliary land 5 is formed at the connection portion 31 between the wiring pattern which constitutes the wire 4 and which is taken inward and the land 13 of the printed wiring board 1 corresponding to the land 13 of the corner portion of the grid array LSI chip 2, a load is applied to the printed wiring board 1 and the concentration of stress of the connection portion 31 when the tensile stress is applied to the connection portion 31 between the land 13 and the wire 4 is moderated, thereby exhibiting the effect that the brake of the wire pattern 4 in the connection portion 31 is prevented.

(Fifth Embodiment)

As shown in Fig.8, a grid array electronic component of

a fifth embodiment is different from the above embodiment in that the auxiliary land 5 is formed in the land 3 connected to the wire pattern 4 which is formed in a direction in which a warpage is generated in the printed wiring board 1 generated in the reflow soldering step of the grid array electronic component (shown with chain line in Fig.8) and in a direction close to the former direction, and the difference will be mainly explained below.

In the fifth embodiment, as shown in Fig.9(A), conveyer frames are disposed in parallel to each other, the printed wiring board 1 is placed on the conveyer frames so that opposite ends of the printed wiring board 1 in a widthwise direction are retained to the conveyer frames, a screen printing board is placed thereon, and cream soldering is printed and applied.

Next, as shown in Fig.9(B), the grid array electronic component 2 is mounted, by a mounter, to an upper surface and/or lower surface of the printed wiring board 1 on which the cream soldering is printed and applied.

Then, as shown in Fig.9(C), the printed wiring board 1 to which the grid array electronic component 2 is mounted is brought into the reflow furnace, and soldering is carried out. At that time, a temperature of the upper surface of the printed wiring board 1 is higher than that of the lower surface of the printed wiring board 1 in the reflow furnace, and arc (U-shape) warpage is generated downwardly by its own weight.

Next, as shown in Fig.9(D), in order to correct the printed wiring board 1 in which the downward arc (U-shape) warpage is generated, a central portion of the printed wiring board 1 is pushed upward from below, and a plurality of portions of the opposite sides of the printed wiring board 1 are pushed downward



from above, this pushing state is maintained for a certain time, thereby correcting the printed wiring board 1 horizontally.

A pin is brought into abutment against a lead of the electronic component of the printed wiring board 1 which was corrected horizontally, individual operations are checked and then, it is assembled into a casing and screwed.

In the fifth embodiment, in the correcting step in which in order to correct the printed wiring board 1 in which the downward arc (U-shape) warpage is generated in the reflow soldering step, a central portion of the printed wiring board 1 is pushed upward from below, a plurality of portions of the opposite sides of the printed wiring board 1 are pushed downward from above, the pushing state is maintained for a certain time, and the printed wiring board 1 is corrected horizontally, since the opposite sides of the printed wiring board 1 which is warped downward are bent downward, a great tensile stress is applied to the connection portion 31 between the land 13 and the wire pattern 4, but the auxiliary land 5 whose width is gradually reduced is formed at the connection portion 31 between the land 3 and the wire pattern 4 which is formed in a direction in which the warpage is generated in the printed wiring board 1 and in a direction close to the former direction, the concentration of stress of the connection portion 31 between the land 3 and the wire pattern 4 is moderated.

According to the grid array electronic component of the fifth embodiment having the above structure, since the tier drops constituting the auxiliary lands 5 are formed at the connection portions 31 (of all the lands 3 on the opposite ends in the lateral direction in Fig.8) between the lands 13 of the printed wiring board 1 corresponding to the lands 3 of the corner portion of

$\frac{1}{\sqrt{\pi}} \int_{-\infty}^{\infty} f(x) \delta(x-a) dx = f(a)$

(Sixth Embodiment)

A grid array electronic component of a sixth embodiment is different from the fifth embodiment in that the present invention is applied to a frame-like grid array LSI chip 2 shown in Fig.10.

In the sixth embodiment, the auxiliary lands 5 are formed on the lands 3 connected to the wiring patterns 4 formed in a direction (shown with chain line in Fig.10) in which warpage is generated on the printed wiring board 1 during the reflow soldering step of the grid array electronic component and in a direction close to the former direction like the fifth embodiment and the same effect is exhibited and thus, explanation thereof will be omitted.

(Seventh Embodiment)

A grid array electronic component of a seventh embodiment is different from the above embodiment in that a relatively small IC chip 21 is disposed on a central portion of a plastic package in which soldering ball grids are disposed on an entire surface in a form of grid like the fifth embodiment (Fig.8) as shown

in Fig.11, and the grid array LSI chip 2 in which the entire upper surface of the plastic package 20 is sealed with resin is mounted on the printed wiring board 1.

In the seventh embodiment, since the rigidity of the plastic package 20 which supports the entire grid array LSI chip 2 is low, it is assumed that a portion of the plastic package 20 of the grid array LSI chip 2 is also warped when the printed wiring board 1 is warped downward in a form of arc (U-shape) in the reflow soldering step.

Therefore, in order to correct the printed wiring board 1 which was warped (that is, it is assumed that stress generated when distortion was corrected when the printed wiring board 1 was mounted to the in-circuit tester is also generated in the connection portion of the wiring pattern of the land and the brake is generated), when the printed wiring board 1 is horizontally corrected by a plurality of resin pins and springs in the in-circuit tester body as shown in Fig.12, since it is assumed that a large stress is applied to the end of the IC chip 21 from the corner portion of the plastic package 20, in the seventh embodiment, the auxiliary land is provided on the connection portion between the land 3 and the wire pattern 4 in this range. The correction can be applied to all of the above embodiments.

According to the grid array electronic component of the seventh embodiment having the above structure, since the auxiliary land 5 is formed at the land 3 located on a position corresponding to the end of the IC chip 21 disposed on the grid array LSI chip 2 of the printed wiring board 1, the concentration of stress of the connection portion 31 between the wire pattern 4 and the land 3 located on the position corresponding to the

end of the IC chip 21, thereby providing the effect that the brake of the wire pattern 4 of the connection portion 31 is prevented.

(Eighth Embodiment)

As shown in Figs.13 to 15, the grid array electronic component of an eighth embodiment is different from the above embodiments in that the auxiliary land 5 is formed at a connection portion 51 around the via hole 14 as a through hole connected to the wire pattern 4 on the inner layer printed wiring board of a multilayer printed wiring board 1 constituting the printed wiring board 1, and the difference will be mainly explained below.

Auxiliary lands 5 whose widths are gradually reduced are formed on the connection portions 31 and 51 of the wire pattern 4 which connects the land 13 and the via hole 14 as shown in Fig.14 on the upper surface of the first layer 101 of the multilayer printed wiring board 1.

As shown in Fig.15, an auxiliary land 5 whose width is gradually reduced is formed on the connection portion 51 which connects the via hole 14 and the wire 4 on the upper surface of the second layer 102 of the multilayer printed wiring board 1.

As shown in Fig.13, the via hole 14 is formed by penetrating the multilayer printed wiring board 1.

According to the grid array electronic component of the eighth embodiment having the above structure, since the auxiliary land 5 is formed at the connection portion 51 around the via hole 14 as the through hole connected to the wire pattern 4 on the inner layer printed wiring board of the multilayer printed wiring board constituting the printed wiring board 1, the

concentration of stress of the connection portion 51 between the wire pattern 4 and the through hole 14 on the inner layer printed wiring board of the multilayer printed wiring board when a load is applied to the multilayer printed wiring board 1 is moderated, thereby exhibiting the effect that the brake of the wire pattern 4 in the connection portion 51 is prevented.

Further, according to the grid array electronic component of the eighth embodiment, since the auxiliary lands 5 whose widths are gradually reduced are formed on the connection portions 31 and 51 of the wiring patterns 4 which connect the land 13 and the via hole 14 as shown in Fig.14 on the upper surface of the first layer 101 of the multilayer printed wiring board 1, the concentration of stress of the connection portions 31 and 51 of the wire pattern 4 which connects the land 13 and the via hole 14 when a load is applied to the multilayer printed wiring board 1 is moderated, thereby exhibiting the effect that the brake of the wire pattern 4 of the connection portion 51 is prevented.

The preferred embodiments of the present invention, as herein disclosed, are taken as some embodiments for explaining the present invention. It is to be understood that the present invention should not be restricted by these embodiments and any modifications and additions are possible so far as they are not beyond the technical idea or principle based on descriptions of the scope of the patent claims.

Although the fan-like and semi-circular auxiliary lands are explained in the above embodiments, the present invention is not limited to those, and as shown in Figs.16, an auxiliary land comprising parallel lines and a tapered portion (Fig.16(A)), an auxiliary land comprising a projected arc portion (Fig.16(B)),

an auxiliary land comprising a recessed arc portion (Fig.16(C)) and the other modes can also be employed.

Although the via hole 14 is formed by penetrating the multilayer printed wiring board 1 as one example in the eighth embodiment, the present invention is not limited to this, and the via hole 14 may be formed so that it penetrates only the first layer of the multilayer printed wiring board 1 or an arbitrary layer thereof as shown in Fig.17.

The auxiliary land is formed on the land of the printed wiring board at a portion corresponding to a portion where an excessive tensile stress of the grid array LSI chip is applied when a load is applied to the printed wiring board in the above embodiment, the present invention is not limited to this, and when there exist a plurality of portion where excessive tensile stress of the grid array LSI chip is applied, or when the portions are changed, or when the portion is in wide range, a mode in which the auxiliary land is formed at an entire land including the entire edge or interior of the grid array LSI chip can also be employed.

Although the opposite ends of the printed wiring board in its widthwise direction are supported by the conveyer frame in the reflow soldering step as one example in the fifth embodiment, the present invention is not limited to this, and it is possible to employ a mode in which the printed wiring board is supported by a mesh-like supporting through which heat and airflow can circulate or pass or by a supporting body in which a large number of supporting pins are embedded, and warpage and distortion of the printed wiring board are prevented from being generated.

an auxiliary land is formed at a connection portion of said land connecting a wiring pattern at a portion where an excessive tensile stress is applied between said lands on the printed wiring board corresponding to said grid array LSI chip and said wiring pattern as said wire.

said auxiliary land is formed at said land located on at least a portion where an excessive tensile stress as compared with another portion of the printed wiring board is applied when a load is applied to said printed wiring board.

said auxiliary land is formed at said land located on a portion corresponding to a corner portion of said grid array LSI chip in said printed wiring board.

said auxiliary land is formed at the land located on a portion corresponding to an end of an IC chip disposed in said grid array LSI chip in said printed wiring board.





9. The grid array electronic component according to claim 3, wherein

said auxiliary land is constituted so that an average value of a connection cross section area of a land closer to the printed wiring board corresponding to the land closer to an end of the corner portion of said grid array LSI chip becomes larger.

10. The grid array electronic component according to claim 2, wherein

said auxiliary land is formed at a connection portion around a through hole connected to the wiring pattern on an inner layer printed wiring board of a multilayer printed wiring board constituting said printed wiring board.

11. The grid array electronic component according to claim 3, wherein

said wiring pattern connected to said land formed with said auxiliary land of said printed wiring board corresponding to a corner portion of said grid array LSI chip is connected to a connection portion formed with an auxiliary land of a via hole on said printed wiring board.

12. A wire strengthening method of a wire which connects a printed wiring board constituting a grid array electronic component and a grid array LSI chip mounted to the printed wiring board, wherein

an auxiliary land is formed at a connection portion between said wire and a land on said printed wiring board corresponding to a land of a corner portion of said grid array LSI chip, thereby strengthening said connection portion of said wire.

13. The wire strengthening method according to claim 12 wherein said connection portion of said wire is strengthened by forming the auxiliary land at said connection portion of said wire of a via hole on said printed wiring board.

14. A producing method of a grid array electronic component for connecting a printed wiring board constituting a grid array electronic component and a grid array LSI chip mounted to the printed wiring board to each other through a wiring pattern, wherein

the grid array electronic component having a strengthened connection portion of said wiring pattern is produced by forming an auxiliary land at a connection portion between said wire and a land on said printed wiring board corresponding to a land of a corner portion of said grid array LSI chip.

15. The producing method of a grid array electronic component according to claim 14, wherein

the grid array electronic component having the strengthened connection portion of said wire is produced by forming the auxiliary land at the connection portion of the wire and the via hole on the printed wiring board.

16. (Added) A grid array electronic component in which a grid array LSI chip having a large number of lands connected to a large number of lands through connecting means, said latter lands are connected to a wire of a printed wiring board, wherein

an auxiliary land whose connection cross section area is increased is formed on a connection portion of said land

connecting a wiring pattern at a portion where an excessive tensile stress is applied in a producing step between a land in a printed wiring board corresponding to said grid array LSI chip and said wiring pattern which is taken outward to be connected to a via hole as said wire.



FIG. 1

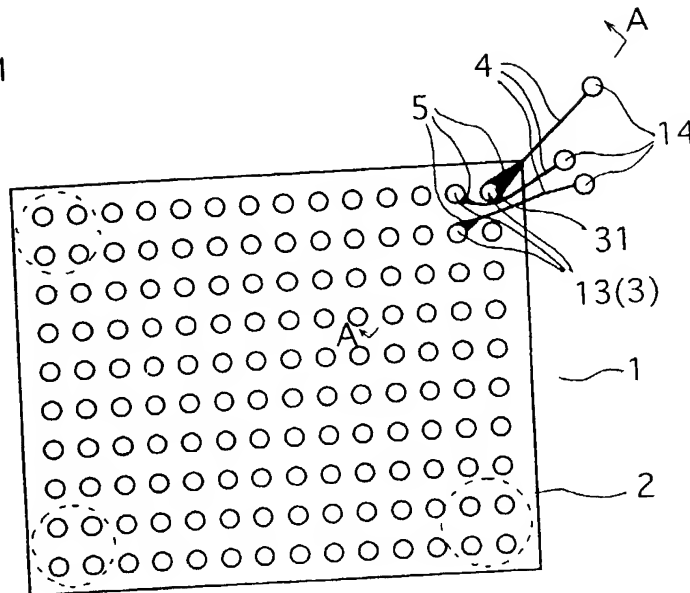
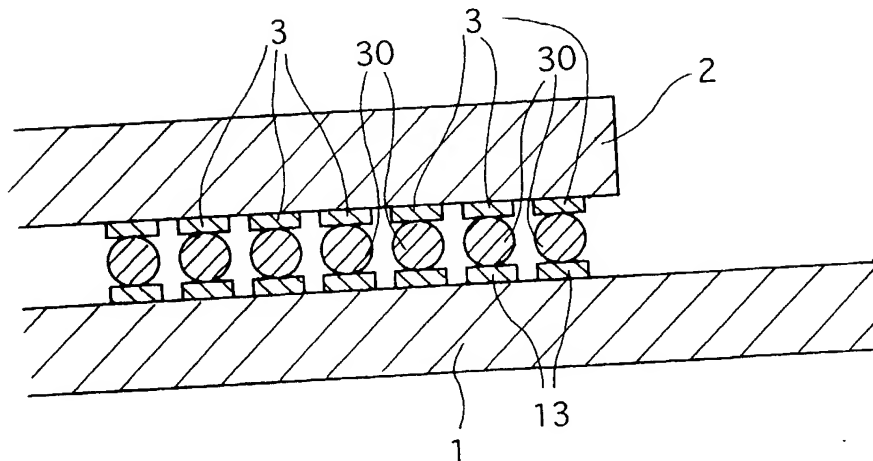


FIG. 2





The diagram illustrates a multi-layered structure with a grid of nodes (circles) and wavy lines (fibers) passing through them. The nodes are arranged in a grid, with some nodes highlighted by wavy lines. The labels 1, 2, 3, 4, 5, 13(3), and 31 indicate different components or layers. A dashed horizontal line is drawn across the middle of the grid.

FIG. 7

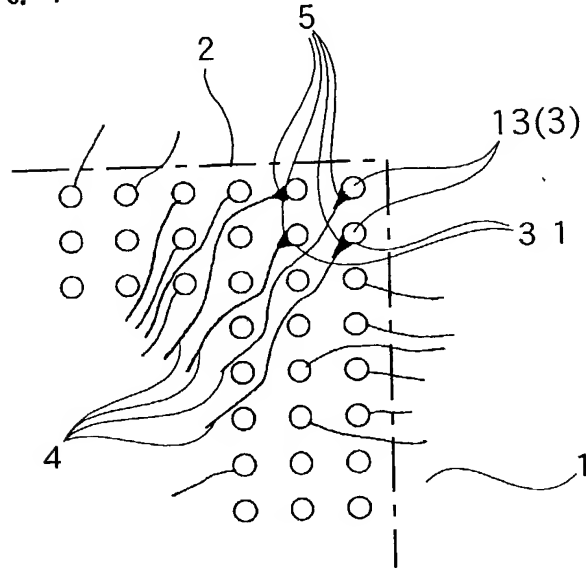
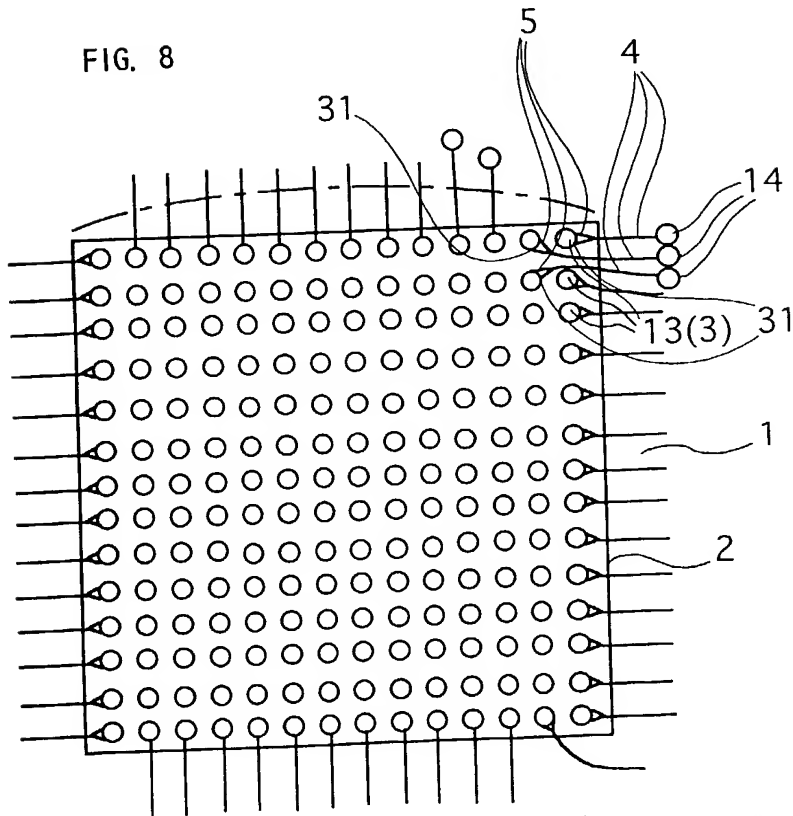


FIG. 8





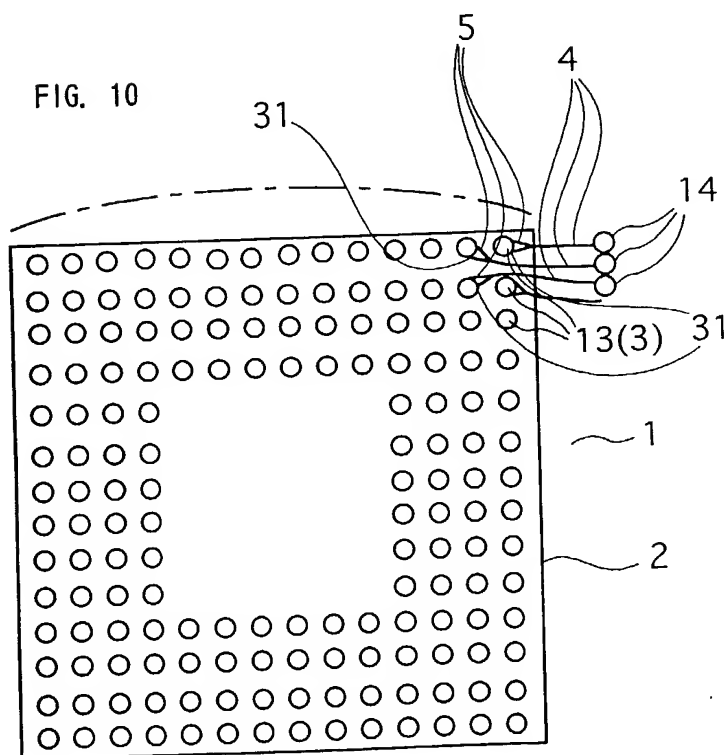
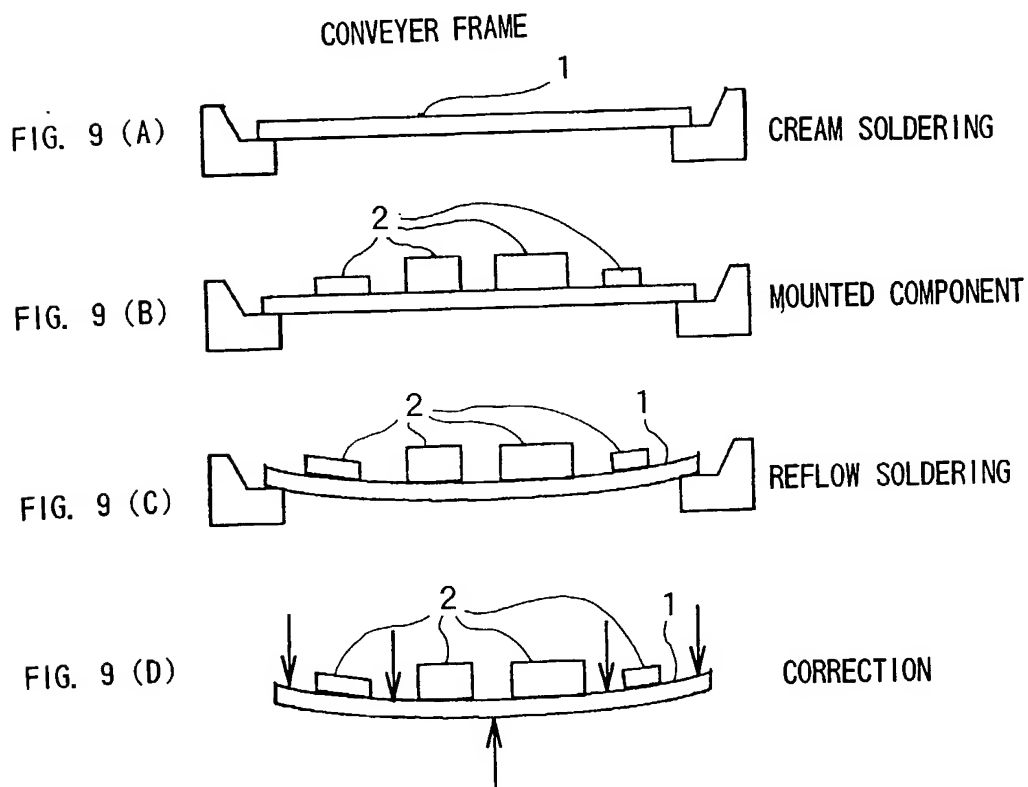




FIG. 13

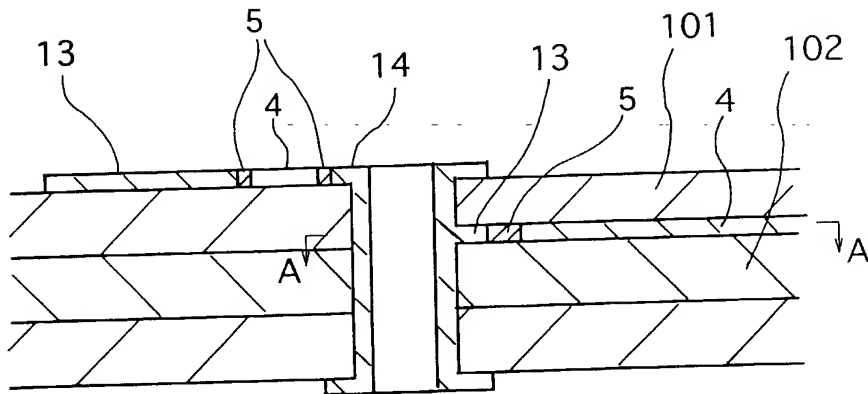


FIG. 14

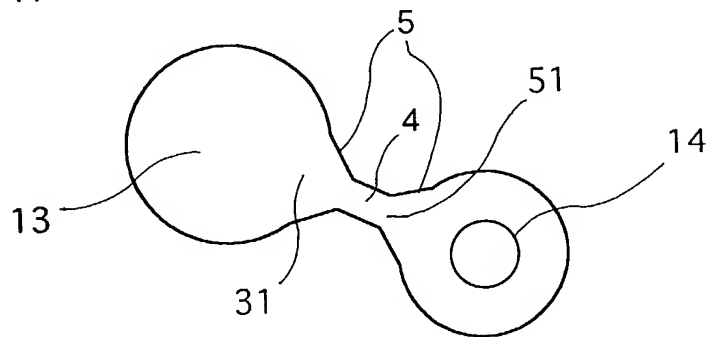


FIG. 15

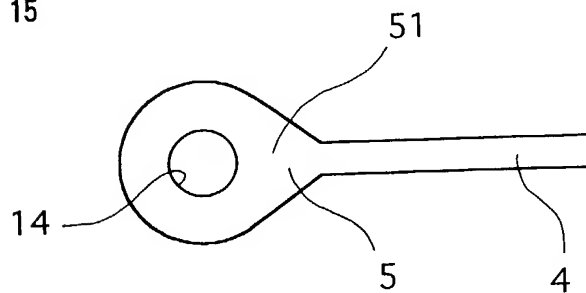


FIG. 16 (A)

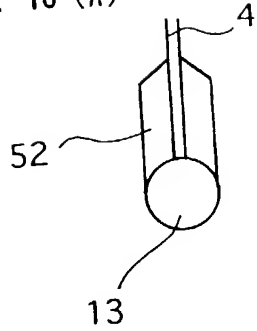


FIG. 16 (B)

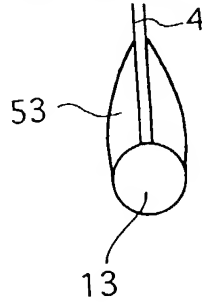


FIG. 16 (C)

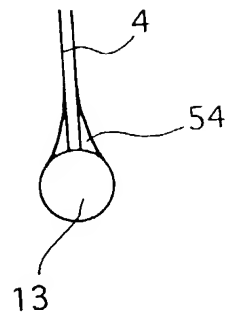


FIG. 17

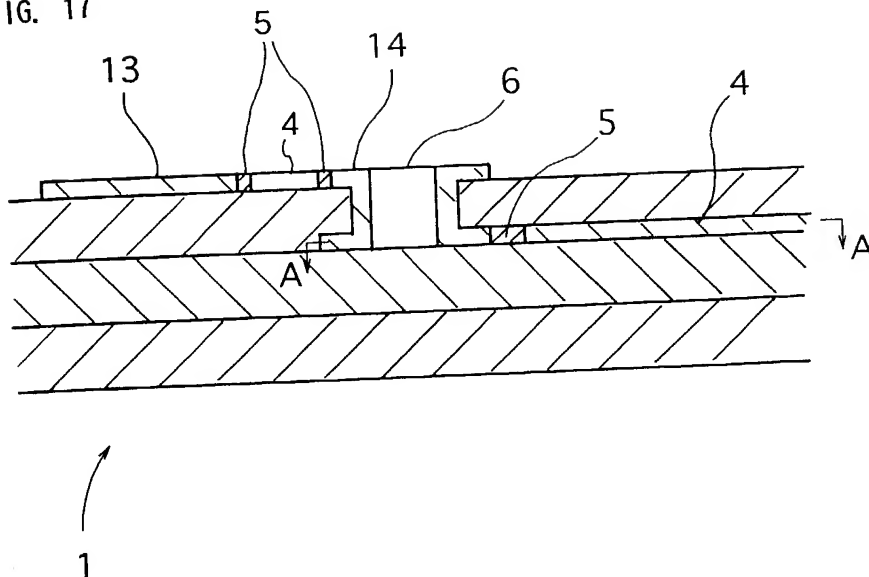


FIG. 18 (A)

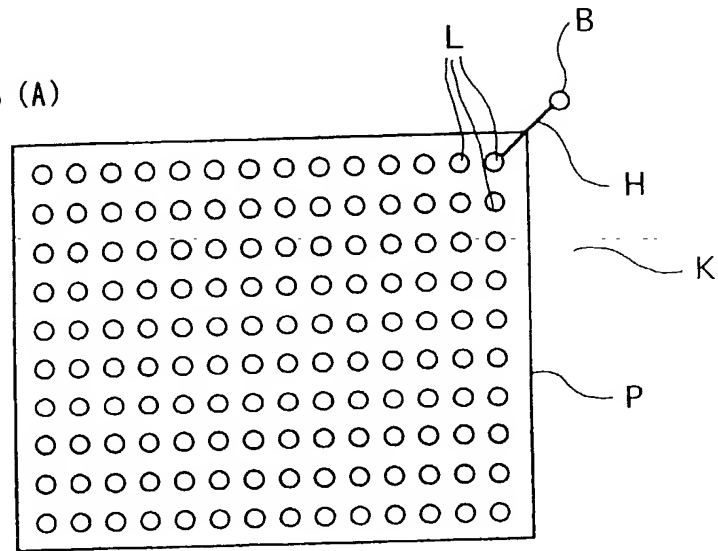


FIG. 18 (B)

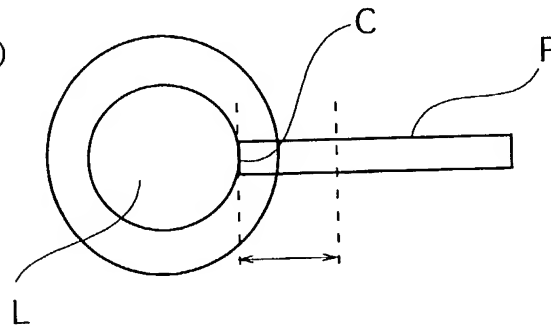


FIG. 19

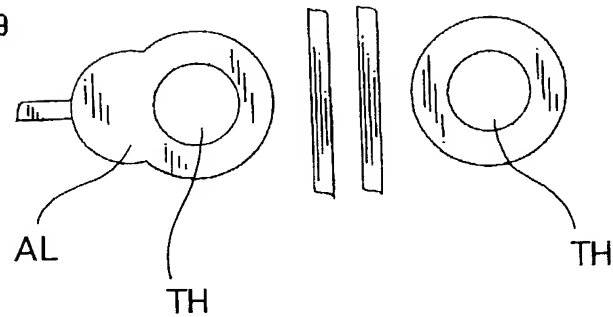


FIG. 20

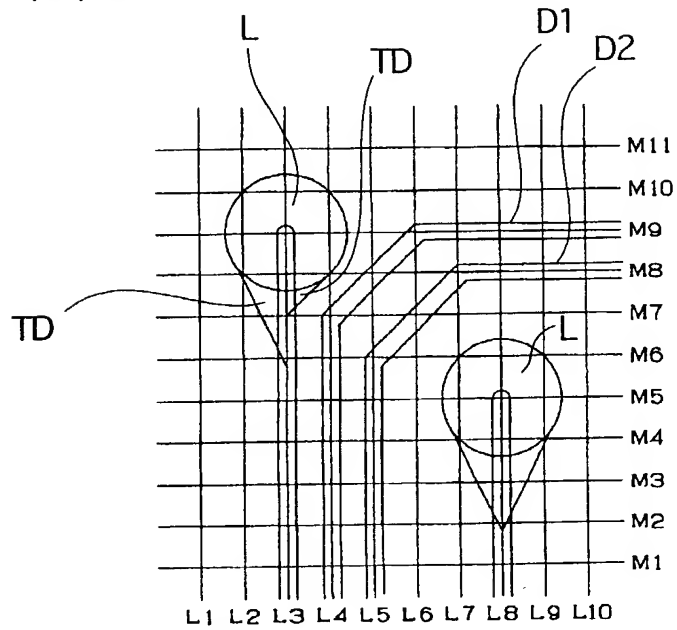
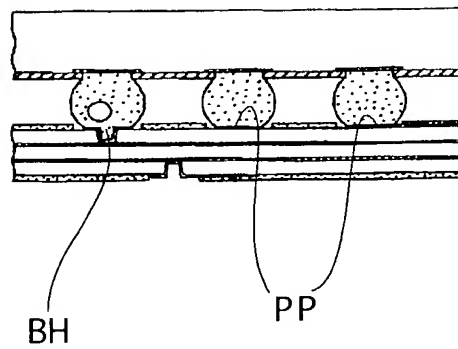


FIG. 21



## Declaration and Power of Attorney For Patent Application

## 特許出願宣言書及び委任状

## Japanese Language Declaration

## 日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

GRID ARRAY ELECTRONIC COMPONENT,

WIRING-STRENGTHENING METHOD AND

PRODUCING METHOD THEREOF

上記発明の明細書は、

the specification of which

☐ 本書に添付されています。

☐ is attached hereto.

☐ \_\_\_\_月\_\_\_\_日に提出され、米国出願番号または特許協定条約国際出願番号を\_\_\_\_とし、  
(該当する場合) \_\_\_\_に訂正されました。

☒ was filed on September 21, 2000  
as United States Application Number or  
PCT International Application Number  
PCT/JP00/06462 and was amended on  
\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

# Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条 (a) - (d) 項又は365条 (b) 項に基づき下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365 (a) 項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

## Prior Foreign Application(s)

外国での先行出願

11-268063 (Pat.)

(Number)  
(番号)

Japan

(Country)  
(国名)

(Number)  
(番号)

(Country)  
(国名)

私は、第35編米国法典119条 (e) 項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条 (c) に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じているところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

## Priority Claimed

優先権主張

☒ ☐  
Yes No  
はい いいえ  
☐ ☐  
Yes No  
はい いいえ

22/09/99

(Day/Month/Year Filed)  
(出願年月日)

(Day/Month/Year Filed)  
(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)  
(現況：特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)  
(現況：特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



**Japanese Language Declaration**  
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。  
(弁護士、または代理人の指名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (list name and registration number)



**022850**

書類送付先

Send Correspondence to:



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国籍		Citizenship Japanese
郵便の宛先		Post Office Address Same as above

(第三以降の共同発明者についても同様に記載し、署名すること)

(Supply similar information and signature for third and subsequent joint inventors.)